In the Specification

Please replace the paragraph beginning on page 6, line 17 with the following amended paragraph:

Preferred embodiments of the invention are well described with the aid of FIGS. 7a-16b. Methods for forming a floating gate structure in which the floating gate is self-aligned to the diffusion according to preferred embodiments of the invention are advantageously described with reference to FIGS. 11a-20b, of which FIGS. na, n=11-20 present top views and FIGS. nb, n=11-20 show cross-sectional views. FIGS. 11a and 11b show the structure just before the etching steps to form isolation regions. To arrive at this stage, a gate insulator layer, 38, which preferably is a grown gate oxide layer of thickness about 90 Angstroms, is formed over the surface of a semiconductor region, 40, which preferably is a crystalline silicon region. A conductive layer, 42, which is preferably a conductive polysilicon layer about 600 Angstroms thick, and an insulator layer, 44, which is preferably a silicon nitride layer about 1600 Angstroms thick, are successively formed over the gate insulator layer. In most preferred embodiments of the invention a hard mask layer, 46, which preferably is an oxide layer deposited to a thickness of about 500 Angstroms, is deposited over the insulator layer. Preferred embodiments of the invention could not have this layer, whose purpose is to protect the underlying insulator layer, 44, during the etching of the semiconductor region, 40, in forming the STI trenches. In case the hard mask layer is not used, an etchant with high selectivity for semiconductor 40 to insulator 44 is required for etching the trenches. Next the hard mask layer, the insulator layer, the conductive layer and the gate insulator layer are patterned into parallel stripes whose direction is denoted the horizontal direction and the direction perpendicular to the stripes is denoted the vertical direction. Forming a photoresist layer and patterning the photoresist layer into parallel stripes, 48, and successively etching the hard

mask layer, the insulator layer, the conductive layer and the gate insulator layer preferably accomplishes this patterning. At this stage, before the photoresist stripes are removed, the structure is as depicted in FIGS. 12a and 12b. The process step that follows the patterning, which is after removal of the photoresist stripes in most preferred embodiments of the invention, is crucial since it enables fabrication of a self-aligned floating gate to diffusion structure without the deleterious affects found in traditional methods. A spacer insulator layer is deposited, which in preferred embodiments of the invention could be about 200 Angstroms of nitride. An etching step follows producing the sidewall spacers 50, which protect the polysilicon sidewalls, 52, from being oxidized during liner oxidation. Next the semiconductor region is etched to produce the shallow trench isolation (STI) regions, 54. It is now safe to form the trench liner layer, 56, which in most preferred embodiments is an oxide layer grown to a thickness of about 250 Angstroms. The thickness of the trench liner layer determines the width of the active regions, which is the width of the semiconductor region, at its surface, between the STI regions and the thicker the trench liner layer, the narrower the active region. Since the sidewall spacers, 50, protect the conductive layer, 42, the conductive layer is not oxidized and it therefore extends beyond the active region. Protection is thus provided to the active region and the defects generated in traditional methods; i.e., conductive layer residue and semiconductor region damage; consequently do not occur in the methods of the invention. Because the conductive layer is not oxidized there is no rounding of the conductive layer and therefore there is no process related impact on the coupling ratio. After depositing an insulator filler layer, which preferably is an HDP oxide layer about 6500 Angstroms thick, a planarization step, which in preferred embodiments of the invention is a CMP step, is performed to achieve the structure shown in FIGS. 16a and 16b, where region 60 is the filled STI region after CMP. An etching step is now

performed, which preferably is an oxide dip etch step, to achieve the structures shown in FIGS. 17a and 17b. Removing the insulator layer, 44, and the sidewall spacer layer, 50, gives rise to the structure depicted in FIGS. 18a and 18b. Edges of the semiconductor region, 64, are in the methods of the invention completely covered by the conductive layer, 42, providing protection so that the conductive layer residue and semiconductor region damage consequently do not occur. It remains to complete the formation of the floating gates, which requires an additional patterning of the conductive layer. Preferably, this patterning is accomplished as indicated in FIGS. 19a and 19b. A photoresist layer is formed and patterned into vertical stripes, 66. Etching the conductive layer and removing the photoresist completes the formation of floating gates, 68, as shown in FIGS. 20a and 20b, which are self-aligned to diffusion according to preferred embodiments of the invention.